PICo Digital Signal Processor Design Project

TEAM ADD

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# INTRODUCTION

# In this paper, we will discuss our product of an embedded digital signal processor design in the FreePDK 45nm technology. In hope to win the contract from the Portable Instruments Company (PICo), we designed and implemented a signal processing ALU with required functionalities (Table1) and the best performance we could achieve. The transistor level hierarchical netlist of the entire DSP, Cadence simulations demonstrating proper functionalities of all functions are attached for review.

# DESIGN DESCRIPTION

The Digital Signal Processor consists of an ALU with 8 available functions (Table1) defined by our 3-bit control value, three registers placed after 16-bit inputs and before output, and buffers after inputs and after registers. Shown below is the top level design of our ALU with its inputs/outputs going through 3 registers.

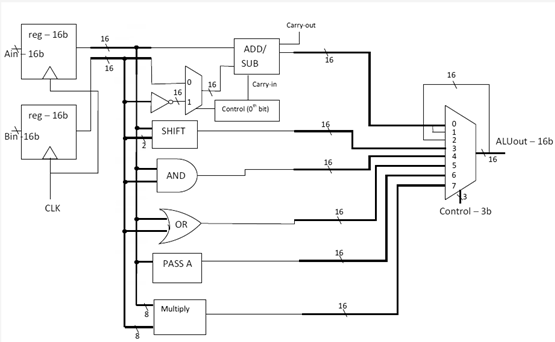


Figure . High Level DSP System

Table . ALU Functions and Descriptions

|  |  |  |
| --- | --- | --- |
| **ALU Functions** | **Description** | **Control** |
| ADD | Out = A + B | 000 |
| SUB | Out = A – B | 001 |
| NOP | No change at Out | 010 |
| SHIFT | Out = A<<B | 011 |
| AND | Out = A & B | 100 |
| OR | Out = A | B | 101 |
| PASS A | Out = A | 110 |
| MULTIPLIER | Out = A (first 8 bits) \* B(first 8 bits) | 111 |

Critical design decisions are discussed in the subsections below.

## Combining ADD and SUB

After testing each path with a different function block, we concluded that the ADD/SUB path has the longest propagation delay and thus it constructs the critical path. Here is how we implemented (combined) ADD and SUB (SUB is ADD with inverted inputs B and Carry-in = 1:

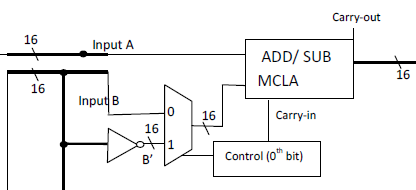


Figure 2. ADD/SUB Implementation

## Modified Carry Look-Ahead Adder

For the ADD/SUB function block, we utilized the **Modified Carry Look-ahead Adder (MCLA)** topology[[1]](#footnote-1).

The simplest binary adder is ripple carry adder[[2]](#footnote-2). It is easy to be understood and implemented. A more complex binary adder is carry lookahead adder (CLA) [[3]](#footnote-3). “It uses the same carry lookahead circuits to construct the higher-bit CLA recursively. It is widely used due to its superior performance over ripple carry adder.”

As discussed by the paper *Fastest Carry Lookahead Adder*, traditional CLA is constructed by XOR, AND, and OR gates. The proposed MCLA uses NAND gates to replace the AND and NOT gates in CLA, it can decrease the cost of CLA and increase the speed of CLA.

Below are the top level schematics of the MCLA that we implemented.

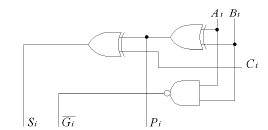


Figure 3. Subcircuit inside a MPFA Block

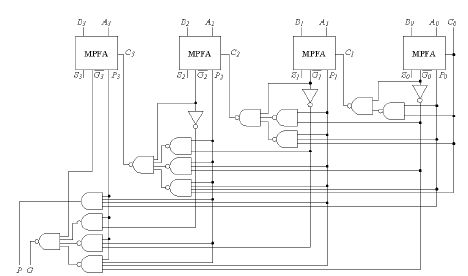


Figure 4. 4-bit MCLA

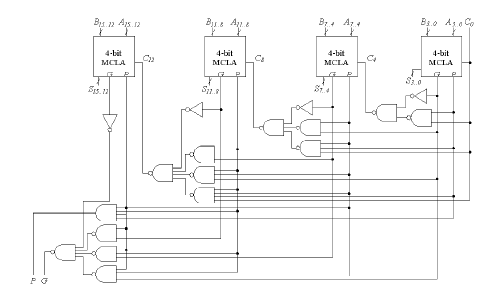


Figure 5. 16-bit MCLA

We chose MCLA over Full Adder and Mirror Adder. Justifications of the utilization of this adder topology will be discussed in Part 3.

## Register Design

For register design, we utilized the **Dynamic C^2MOS Master-slave Positive Edge-triggered Register**[[4]](#footnote-4).

We compared topologies of four registers discussed in the textbook: Static CMOS Master-slave Positive Edge-triggered Register, Dynamic Transmission Gate Edge-triggered Register, C^2MOS Master-slave Positive Edge-triggered Register, and Positive edge-triggered resister in TSPC.

Justifications of the utilization of this register topology will be discussed in Part 4.

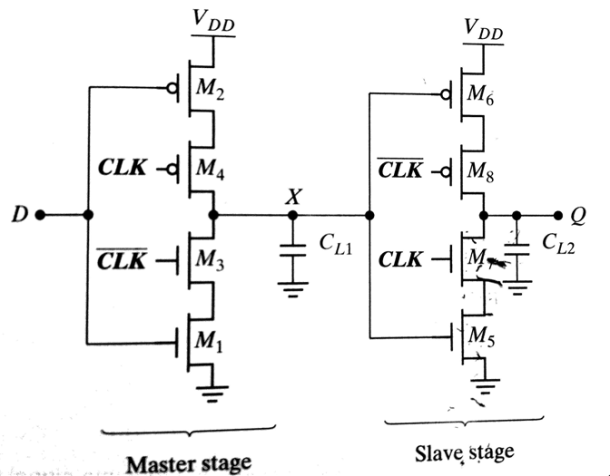


Figure 6. C^2MOS Master-slave Positive Edge-triggered Register

## Vdd Value

We tested the design product using 0.95V, 1V and 1.1V as the voltage supply (Vdd). **0.95V** is the one that gives the smallest metric, while having the design work properly.

## Sizing

To order to minimize the total area, we set all gates not on the critical path to minimum sizes (wn,wp=90n). For transistors on the critical path, they are sized for equal pull-up and pull-down strength. Transistors driving larger load are sized larger. Sizes are shown in the Netlist attached.

# INNOVATION

In order to attain the best performance and minimum metric consumption (Delay^2\*Power\*Area), we did the following:

1. Change/optimize components topologies
   1. Combine ADD and SUB into one function block with inverted inputs. It saves area and power consumption, but adds a little more delay.
   2. Combine the ALU MUX select bit 0 with the ADD/SUB block MUX select line and the carry in input (Figure2).
   3. Use Modified Carry Lookahead Adder topology. Its delay is tested to be about ½ of that of the Full Adder. However, it costs area since there are more gates, and adds a little bit more power.
   4. Utilize Dynamic C^2MOS Master-slave Positive Edge-triggered Register topology. It is tested that this topology is insensitive to clockskew. It uses a minimum number of transistors thus area, it consumes significantly less power, and it has the minimum delay. However, the tradeoff is that it is less robust and requires buffers at the output to avoid being affected by changes elsewhere in the circuit.
2. Size the elements on the critical path
   1. Minimize sizing for elements not on the critical path. This reduces total area.
   2. Upsize elements on the critical path to obtain the best delay. We sized the transistors to have equal pull-up and pull-down strength. Then, for elements driving big load (fanout), we upsized them to a point where the area does not increase too much, but the delay gets minimized. Because of the complexity of this processor, we did not do hand-calculations for optimal sizing. But through running multiple simulations, we obtained the results that give us the best metric. See attached Netlist for sizing detail. This reduces the worst-case delay, but increases area.
3. Reduce the supply voltage Vdd to obtain the best metric while having all functions work properly. Lower Vdd gives less power but greater delay. Also if it is too low, the circuit does not work properly.

## Design Decision Justification

1. Vdd Value

Table 2. D^2\*P of Same Processor with Different Vdd

|  |  |  |  |
| --- | --- | --- | --- |
| **Vdd** | **0.95V** | **1.0V** | **1.1V** |
| Delay\_wc(s) | 3.40E-10 | 3.20E-10 | 3.0E-10 |
| Active Power(w) | 2.94E-04 | 3.60E-04 | 4.56E-04 |
| D^2\*P | 3.40E-23 | 3.69E-23 | 4.10E-23 |

As shown in the table, 0.95V voltage supply gives the best metric.

1. ADDER Topology

Table 3. Metric of Processor Implementing Different ADDER Topology (vdd=0.95V)

|  |  |  |
| --- | --- | --- |
| **ADD** | **Mirror** | **MCLA** |
| Delay\_wc(s) | 5.00E-10 | 3.40E-10 |
| Power(w) | 2.14E-04 | 2.94E-04 |
| Area(m) | 2.49E-04 | 3.65E-04 |
| Metric(P\*D^2\*A) | 1.33E-26 | 1.24E-26 |

As shown in the table, MCLA gives the better metric. Note we did not put Full Adder here because it is obvious that the Mirror Adder has better performance in terms of the specified metric.

1. Register Topology tested with ideal clock in a separate test circuit (not as part of the processor)

Table 4. Metric of Register of Different Topology

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **REG** | **Static CMOS** | **Dynamic Passgate** | **C^2MOS** | **TSPC** |
| # transistors | 22 | 8 | 8 | 11 |
| Power(w) | 6.28E-5 | N/A | 2.45E-5 | 3.37E-5 |
| Delay\_wc(s) | 2.9E-11 | N/A | 1.5E-11 | 2E-11 |

As shown in the table, C^2MOS gives the better performance in all aspects. Note we did not test Dynamic Passgate’s power and delay here because it is sensitive to clockskew and had bad output.

We chose C^2MOS as the register topology, and then tested it more rigorously. With a non-ideal buffered clock, it still outperformed Static CMOS in every metric.

## Arbitrary Function

Our arbitrary function is an 8-bit multiplier. It takes in two 16-bit inputs, multiplies their first 8 bits and outputs a value up to 16 bits.

We chose regular full adders and Andgates (with minimum sizes wp=wn=90n) to implement the multiplier, since it is the most convenient to implement and there is no requirement on the delay metric. However, this saves area.

Due to the output bit limitation (16 bits in total) of the ALU, the maximum numbers of bits of each input are set to 8. The multiplier then takes the first 8 bits of both inputs (A7-A0, B7-B0) and outputs the multiplication results in 16 bits.

Delay, power, area results of the multiplier is shown in Table5 in 4.2. Simulation results are attached.

# RESULTS

## Metric

Metric = Active Power\*Delay^2\*Area = 2.94E-4W\*(3.4E-10s)^2\*3.65E-4m = **1.24\*10^-26 (m\*s^2\*W)**

## Multiplier Results

Table 5. Results from Multiplier

|  |  |
| --- | --- |
| Delay(s) | 6.00E-09 |
| Power(w) | 1.35E-07 |
| Area(m) | 2.46E-04 |

## Power and Delay Breakdown

For different components in the design, we broke down the power consumption and delay on the critical path to analyze how much each element contributes.

**Table 6. Power (without multiplier) in terms of Ratio of Total Power**

|  |  |
| --- | --- |
| Shift | 7.2% |
| AND | 6.6% |
| OR | 14.3% |
| ADD/SUB | 59.5% |
| NOP | 3.1% |
| pass A | 2.4% |

**Table 7. Percentage Worst-case Delay Ratios for each function (tested in Design Review 2)**

|  |  |
| --- | --- |
| **Operation** | **Worst-Case Delay Ratios** |
| ADD | 119.575 |
| SUB | 120.875 |
| SHIFT | 4.15 |
| AND | 1.0875 |
| OR | 1.15 |
| PASS A | 1 |

For worst case delay use bit pattern A=0xFFFF B=0x0000 -> 0x0001

**Table 8. Delay Breakdown (without multiplier) on Critical Path**

|  |  |  |
| --- | --- | --- |
| Sum Delay (B0->ALUOut ), s | 2.599E-10 | 76.4 % |
| Carry Delay (B0->Cout),s | 1.721E-10 | 50.5% |
| Register Delay1 (Bin-B0) | 1.846E-11 | 5.4% |
| Register Delay2 (Regin->Out) | 1.8458E-11 | 5.4% |

# CONCLUSION

# In this paper, we discussed our product of an embedded digital signal processor design in the FreePDK 45nm technology. We designed and implemented a signal processing ALU with required functionalities for two 16-bit inputs: addition, subtraction, NOP, shifting, AND, OR Pass and multiplication. We obtained the best performance by optimizing ADD/SUB algorithm, adder design, register topology and voltage input. The transistor level hierarchical netlist of the entire DSP, Cadence simulations demonstrating proper functionalities of all functions are attached for review.

# As shown by the top section of delay breakdown, we proved that we chose the correct critical path, and successfully minimized the critical path delay. Also, we worked with the tradeoff between area and delay for different topologies for ADD/SUB, and found the right one with the best performance. Moreover, our design uses the minimum vdd we could use to save power consumption. Overall, our design product meets all the requirements proposed by PICo. We wish to further work with the company under the contract.

# REFERENCES

1. Pai, Y., and Chen, Y. “The Fastest Carry Lookahead Adder”, *IEEE Computer Society.,2004*
2. C. Nagendra, M. J. Irwin, and R. M. Owens, “Area-timepower tradeoffs in parallel adders”, IEEE Transactions on Circuits and Systems II, 1996, vol. 43, pp. 689-702.
3. J. Lim, D. G. Kim, and S. I. Chae, “A 16-bit carrylookahead adder using reversible energy recovery logic for ultra-low-energy systems”, IEEE Journal of SolidState Circuits, 1999, vol. 34, pp. 898-903.
4. J. Rabaey, A. Chandrakasan, and B. Nikolic, “Digital Integrated Circuits – A Design Perspective”, 1995

1. [↑](#footnote-ref-1)
2. [↑](#footnote-ref-2)
3. [↑](#footnote-ref-3)
4. [↑](#footnote-ref-4)